CM712x Audio DSP & CODEC Hub System

Application Note

Jan. 26, 2018

Introduction

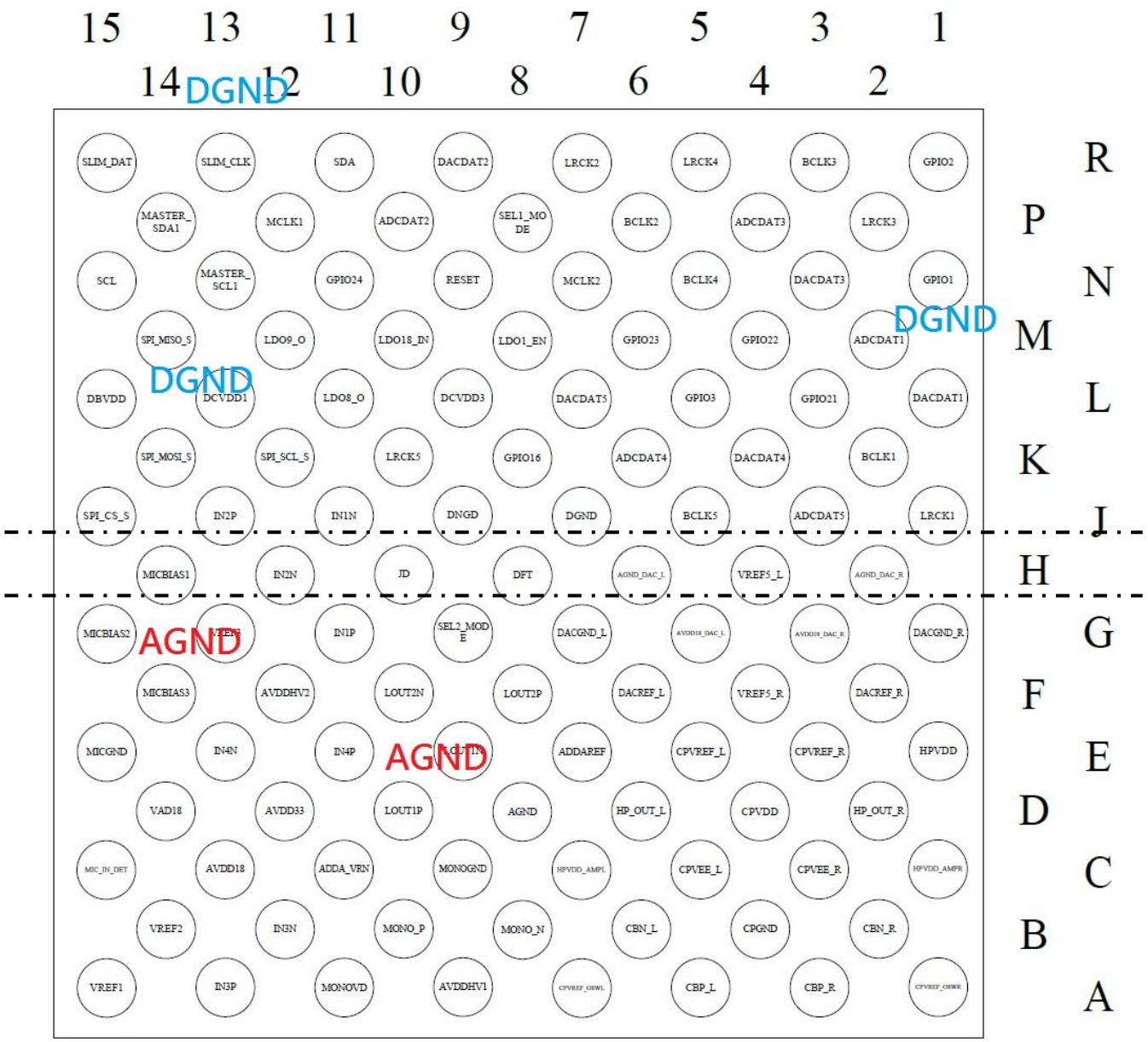
To ensure maximum performance from the CM712x DSP codec, proper component placement and routing are very important. This document includes properly isolating the digital circuitry and analog circuitry.

The effects of ground and supply plane geometry, decoupling/bypassing/filtering capacitors placement priorities, LINK signals, analog power supplies, and analog ground planes.

The layout design of Ground and Supply plane Geometry

Figure.1 shows a top view layout of ground plane for CM712x codec. This layout separates the analog and digital ground planes with a 20 to 40 mils gap. The moat helps to isolate noisy digital circuitry from quiet analog audio circuitry. *The digital and analog ground planes are tied together at one point (Ferrite Bead or 0ohm resistor).*This will be the "drawbridge" that goes across the moat. Similarly, NO SIGNALS WHATEVER are permitted to cross the moat (to do so creates a "slot antenna" radiator which will hammer your PCB layout with crosstalk, and create huge amounts of EMI, totally defeating your purpose).CM712x also supports a charge pump cap-less headphone output. It is better to CPGND to DGND.

For a layout that helps to reduce noise, separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their respective ground planes. Placing analog power coincident with analog ground, and digital power coincident with digital ground (as Figure.2 – right separation). If any portions of analog and digital plane overlap, the distributed capacitance (result from power plane reference to ground plane or signal plane reference to ground plane) between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolated plane (as Figure.2 – wrong separation). The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.



CM712x WLCSP 113 Ball(Bottom View)

Figure1.CM712x ground plane Layout Guide

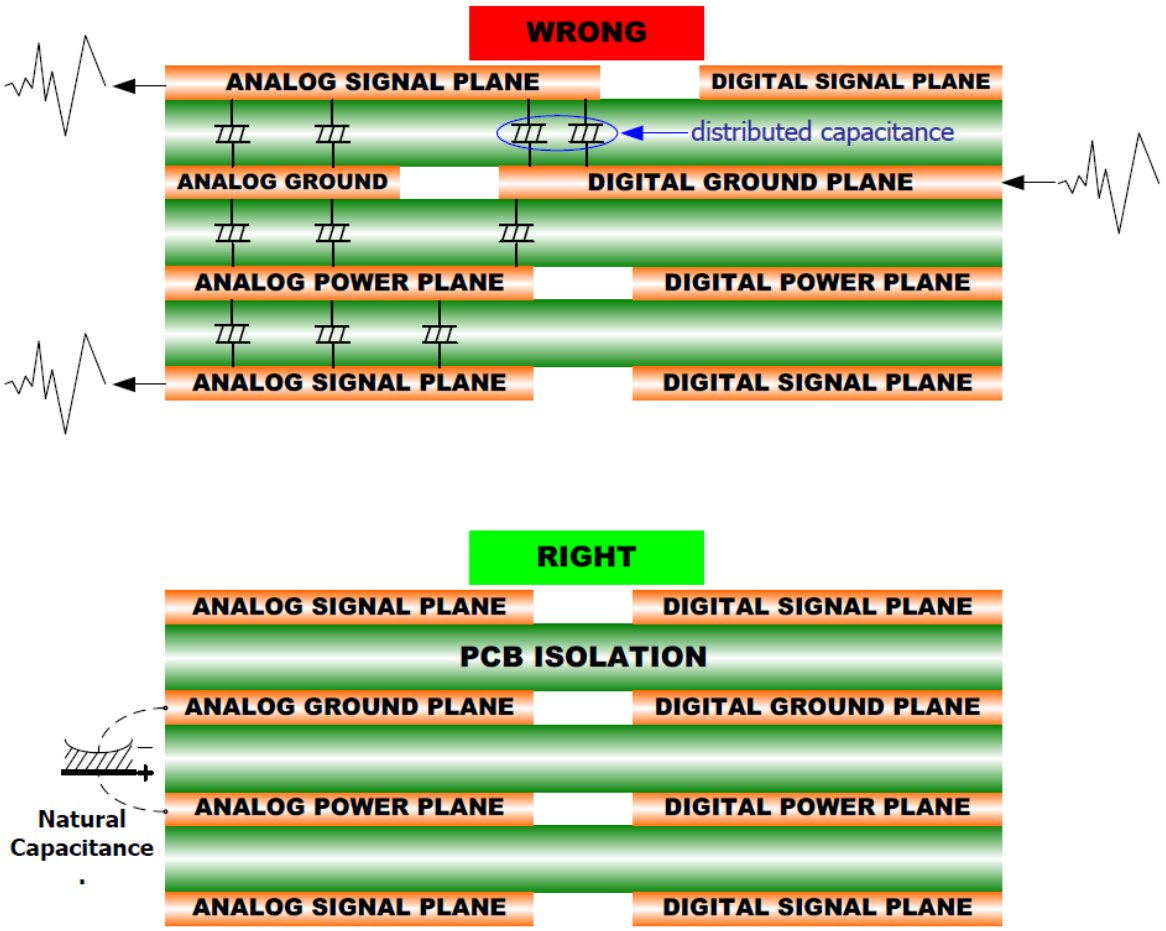


Figure2. Side view of PCB, the right separation of analog and digital plane.

Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise into ground.Commonly, codec generates noise when its internal digital circuitry turns currents on and off. These current changes arise in the power and ground pins for the related section of the codec.The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back into the codec through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the codec and the bypass capacitors when in the operating frequency of the codec. The longer the trace – the greater the inductance. To avoid long-trace inductance effects, use the shortest possible traces for bypass capacitors, with wide traces to reduce impedance. For best performance, use supply bypass leads of less than one-half inch.

In Table1, it shows the priorities of Cmedia CM712x codec capacitor placement

1. Pins with a first – “A” priority components placed around the codecare the bypass caps, which are located as close as possible to the power supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR).
2. The filter capacitors with “B” priority stabilize the reference voltage for internal Ops should be placed close to codec. A good reference voltage is relative to good analog performance.
3. These decoupling capacitors (“C” priority) should be close to the codec pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance. The Table 1 also point out the distribution of codeccapacitor locations and placement priorities.

Table 1.CM712x **codec** capacitor placement priorities

Signal Description	Package Pins	Priority of Close Proximity to DAC Pin Placement of Filter and Decoupling Capacitors
Digital Supply Voltage , DBVDD	L15	A
Digital Supply Voltage , +1.8LDO_IN	M10	A
Digital Supply Voltage , DCVDD1,DCVDD3	L9,L13	A
LDO8_O,LDO9_O	L11,M12	A
AVDD_18_DAC_L/R	G3,G5	A
Analog Supply Voltage, +1.8AVDD18	C13	A
AVDD33,+3.3V	D12	A
AVDDHV1,AVDDHV2	A9,F12	A
MonoVDD	A11	A
CPVDD,HPVDD,HPVDD_AMPL/R	D4,E1,C7,C1	A
Voltage Reference Filter(V_{REF})	A15,B14,G13,H4,F4,E7	B
HP charge pump relative	C3,C5,A5/B6,A3/B2	B
Analog Signal Inputs & Output(Decouple)	G11,J11,J13,H12,A13, B12,E11,E13	C

The trace routing

I. Power Input trace

For the better loading ,the power traces width are better to correspond to the suggestion as below:

1.LDO18_IN,LDO8_O,AVDD18,AVDD18_DAC_L,AVDD18_DAC_R,VAD18,DBVDD,HPVDD, HPVDD_AMPL,HPVDD_AMPR>= 10mils

2. CPVDD>=15mils

3. AVDD33>=15mils

4. AVDDHV1,AVDDHV2, >=20mils

II. Analog Input & Output signal trace

For reaching the best audio quality, some guide line should be obeyed.

1. To avoid a cross-talk issue result from having no enough space between channels or input/output traces. The cross-talk may affect the performance of analog signal, especially the IN1 , IN2 ,IN3 , IN4 . In Figure 3, the isolation between IN2P/N and IN1P/N are routing as wider as possible (L at least 40mils).

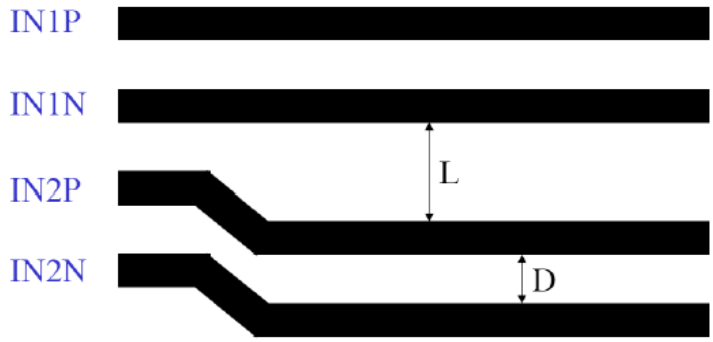


Figure3.The routing for analog input(L>60mils , D<=10mils)

2. The IN1 and IN2 microphone input signals are more sensitive than the other signals. These two signals may route to the other layer if possible, and we can see that in Figure 4.In Figure 4, IN2 input signal are routing on layer2. But IN1 microphone input are routing on layer1 between codec and phone jack input.

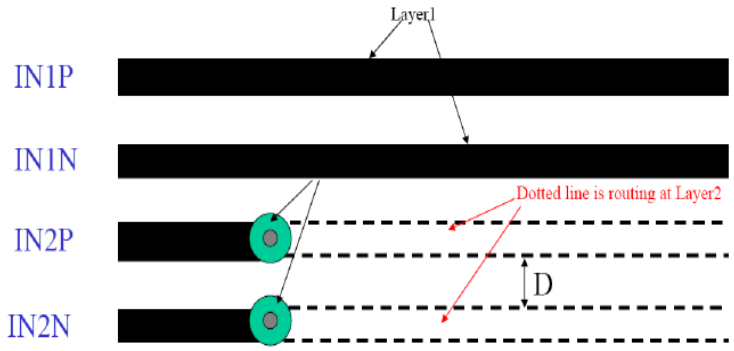


Figure4.The special routing for mic input signal(D<=10mils)

3. For better audio performance, analog input & output traces width should be as wide as possible.
   IN1P/IN1N ,IN2P/IN2N, IN3P/IN3N , IN4P/IN4N>8mils (10mils is better)
   LOUT1L/LOUT1R,LOUT2L/LOUT2R >10mils (15mils is better)
   HPO_L/HPO_R > 15mils (20mils is better)
   MonoP/N > 15mils(20mils is better)

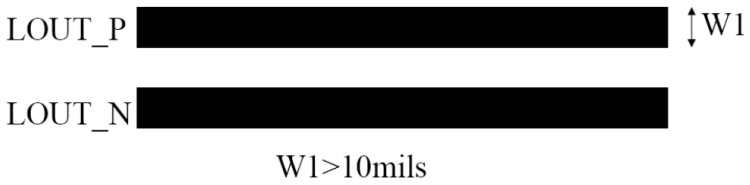


Figure 5.The special routing for LOUT signal(W1>10mils)

4. The signal length from codec to input/output connector should be as short as possible.

5. To improve cross-talk performance, some rules must to follow
   - CPVREF_L/R & CPVREF_OSWL/R need to be short to jack AGND as close as possible.
   - The width of CPVREF trace has to be as wide as possible. Width wider than 10 mils is suggested.

6. The width between differential pair should be small(D<=10mils)

7. The digital microphone clock (CLK) Trace
   The digital microphone is not sensitive to the ground plane. The normal operation clock of digital microphone is around 1MHz to 3MHz bit rate, a long trace causes a slow rising time that makes CLK waveform is deformed, or different of trace length between CLK and DATA

signal cause skew variation, both will influence digital microphone performance. The CLK and DATA signals should be routed by using at least 5-mil width of trace and 5-mil space between each other, and keep both traces have the same length.

8. The space between each trace should better to be filled with copper which connect to analog ground.

9. MCLK,BCLK,LRCK,ADCDAT,DACDAT of I2S signals should keep the same length and then as short as possible.

The suggestion of layout plane

Ground layer:

Please separate digital signals and analog signals, then connect digital signals and analog signals by resistances.

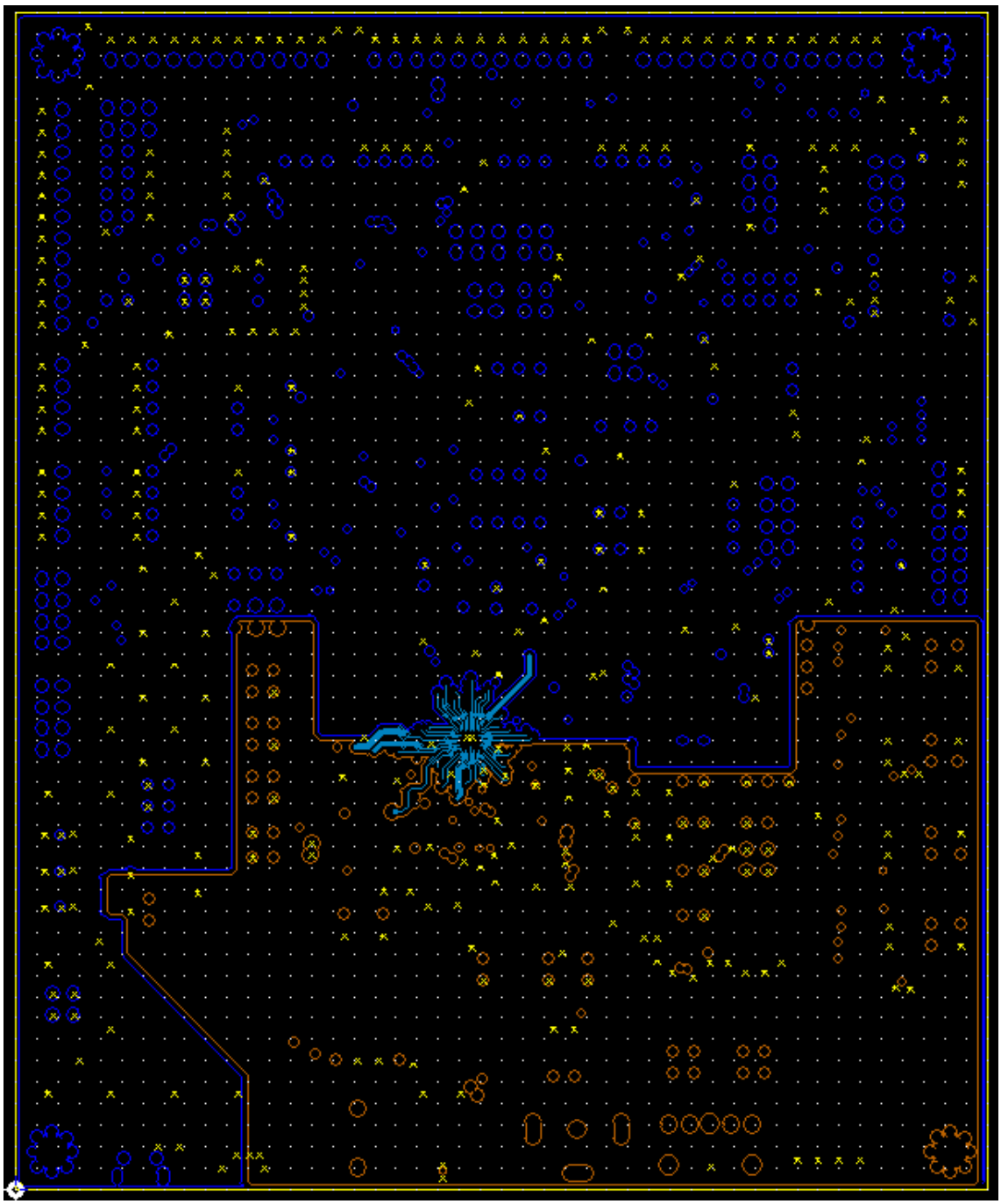


Figure 6.The Ground layer I

Power layer:

Please separate power plane to five parts for 5V，3.3V，2.5V，1.8V and 1.2V。

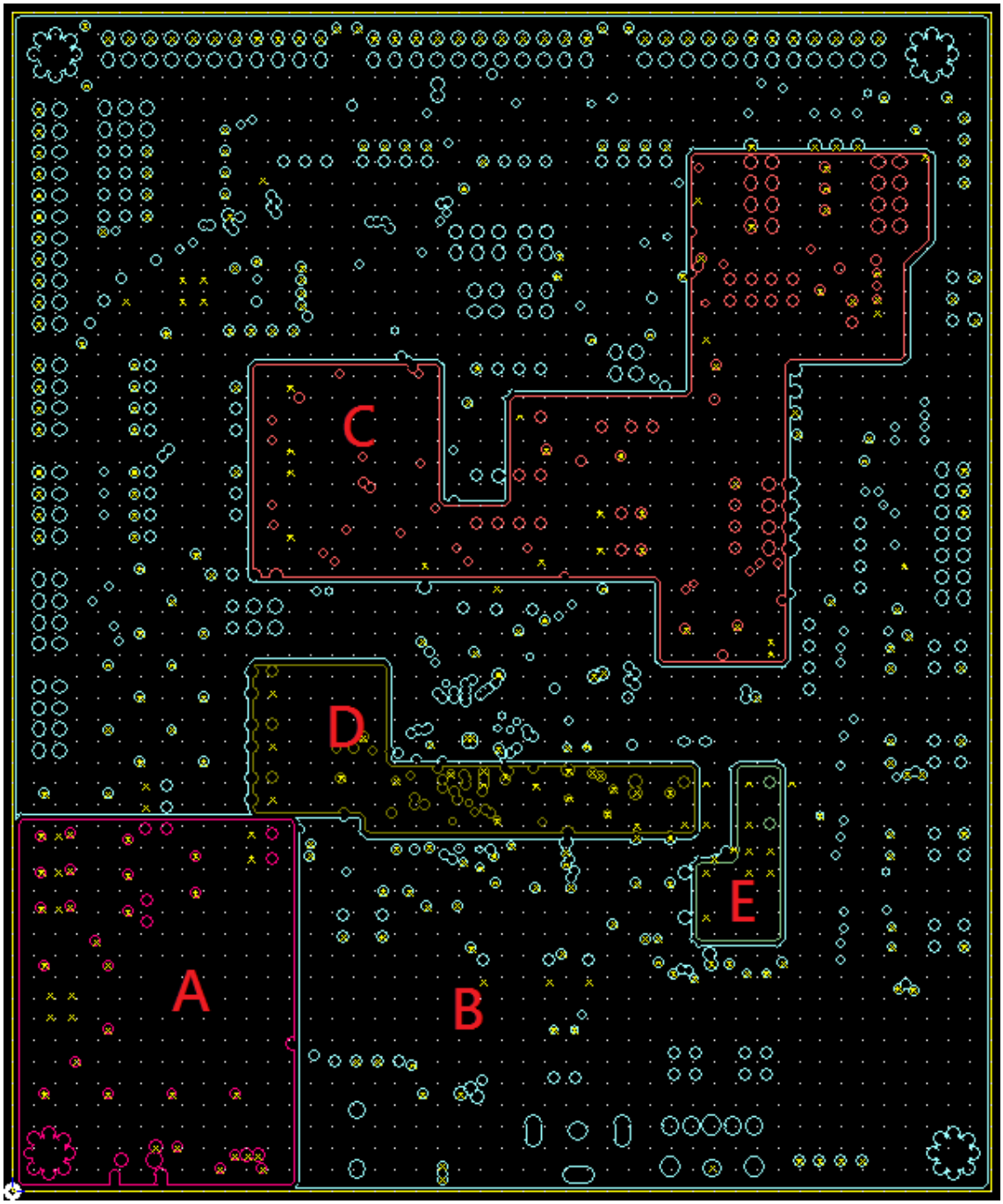


Figure 7.The Power layer

The reference of all layers of CM712x

Layer 1:Singal layer Ⅰ

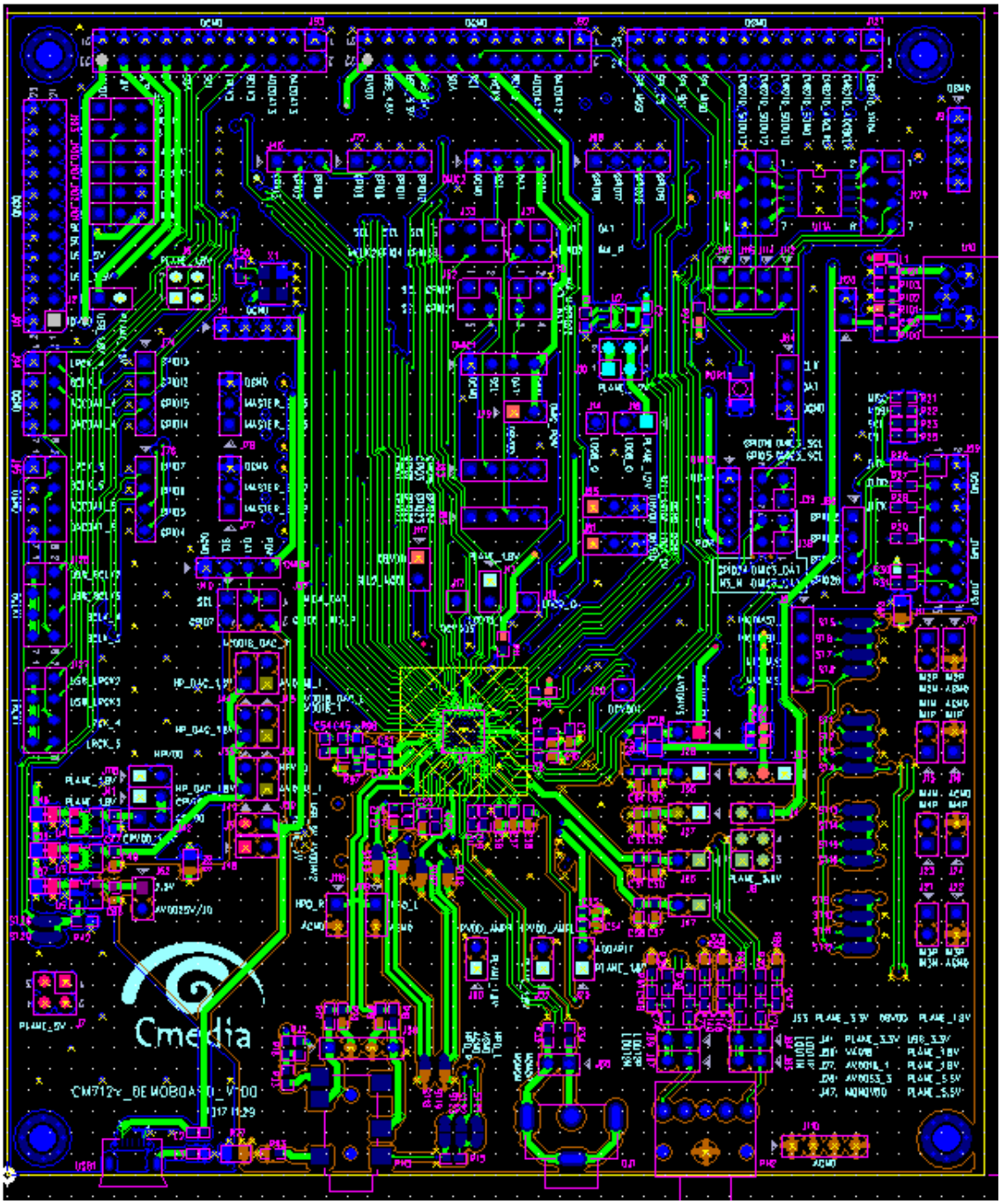


Figure 8.The TOP layer

Layer 2: Ground Layer Ⅰ

Please see Figure 6.

Layer 3: Signal Layer Ⅱ

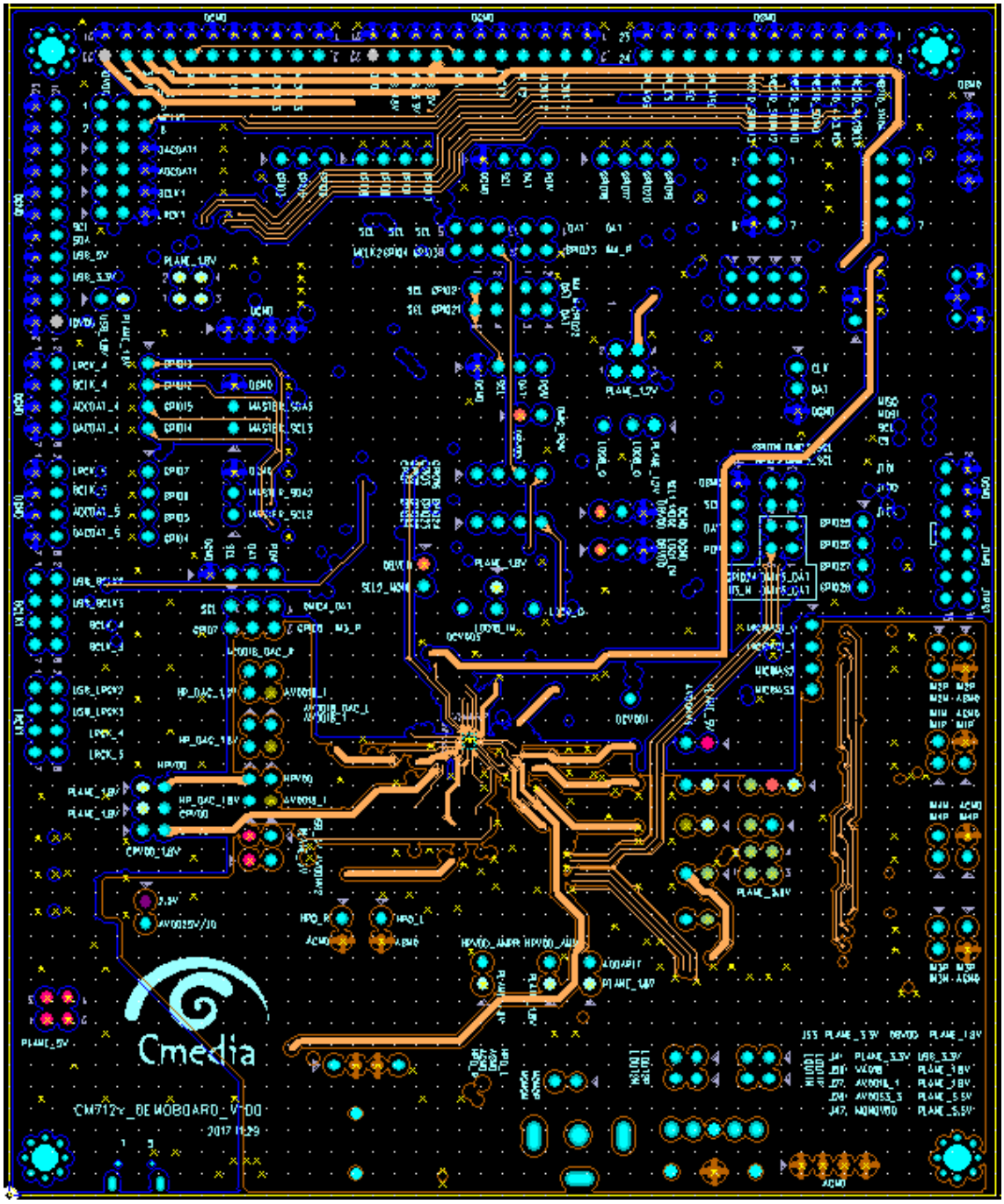


Figure 9.The 3rd. Layer

Layer 4: Power Layer

Please see Figure 7.

Layer 5: Ground Layer Ⅱ

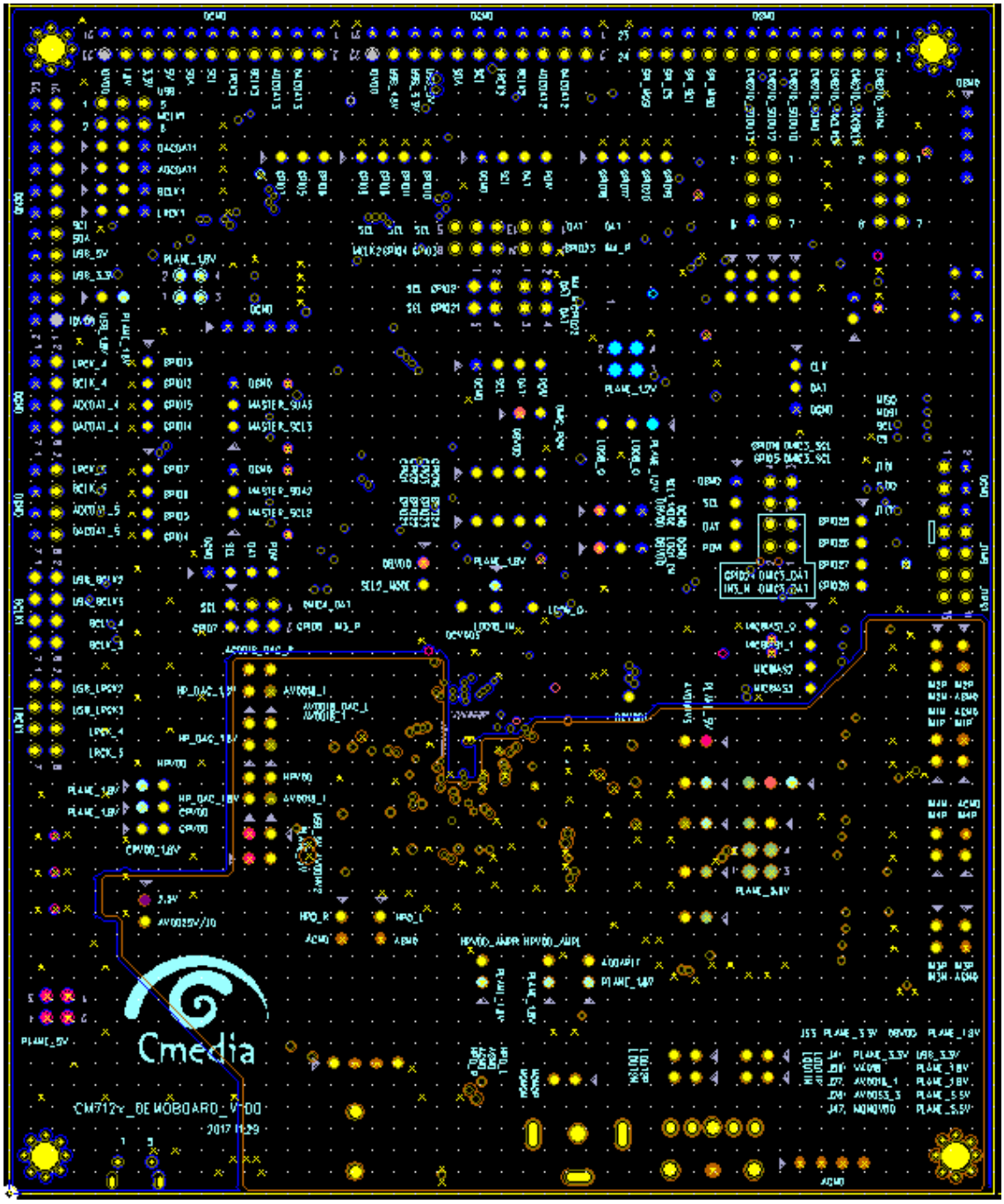


Figure 10.The 5th. Layer

Layer 6: Signal Layer Ⅲ

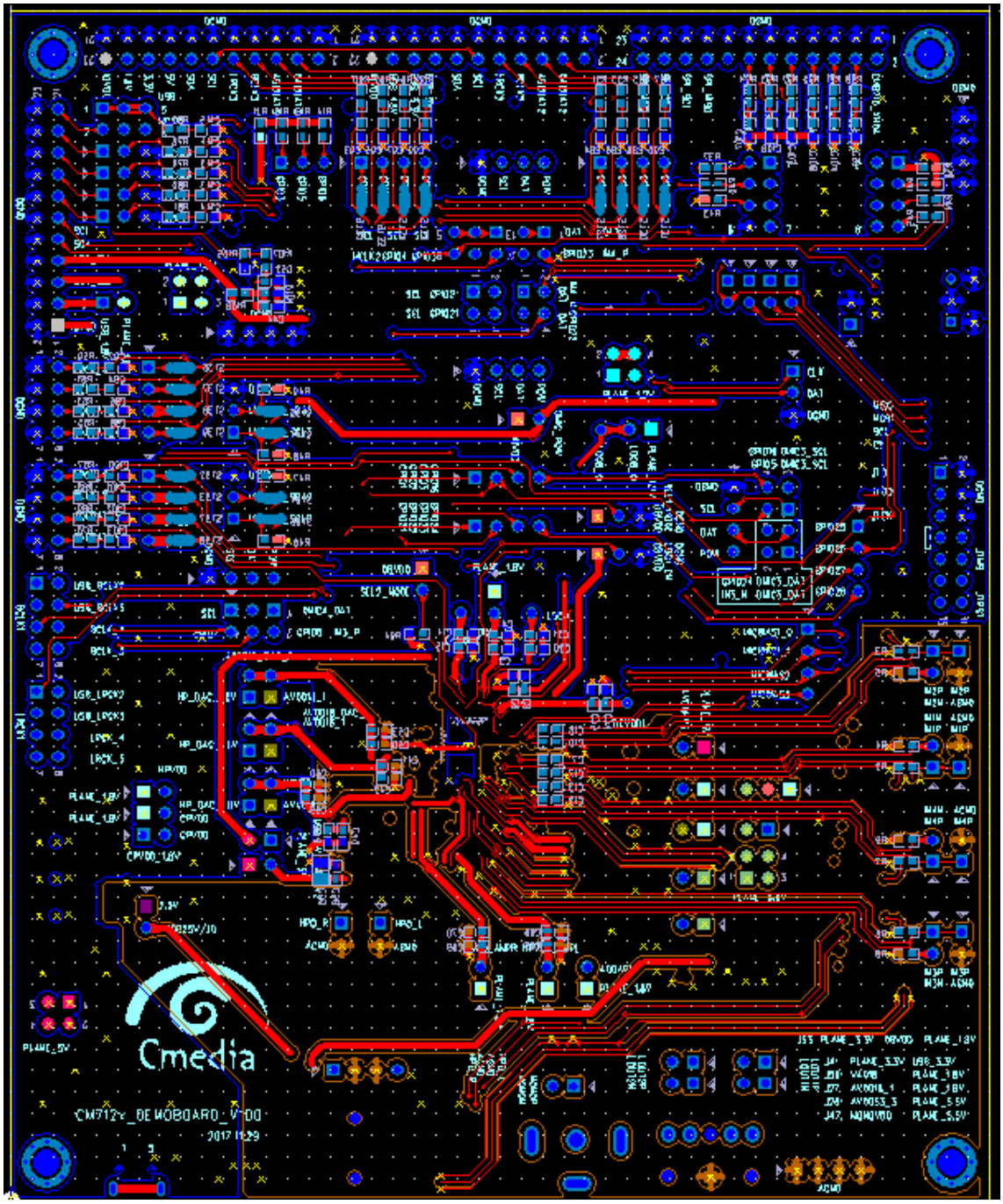


Figure 11.The 6th. Layer